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APPLICATION NO. FILING DATE		ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,969	11/06/2001		Soubhi Abdulkarim	42390P12804 2765	
45459	7590	12/13/2005		EXAM	INER
GROSSM	AN, TUC	KER, PERREAUI	CHEN, TSE W		
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MINNEAPOLIS MN 55402				2116	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)					
	10/005,969	ABDULKARIM, SOUBHI					
Office Action Summary	Examiner	Art Unit					
	Tse Chen	2116					
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the	correspondence address					
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 16(a). In no event, however, may a reply be ting 17 iiii apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. mely filed in the mailing date of this communication. ED (35 U.S.C. § 133).					
Status							
1) Responsive to communication(s) filed on 11 Oc	ctober 2005.						
	action is non-final.						
·=	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under E	•						
Disposition of Claims							
4)⊠ Claim(s) <u>1,4-8,11-14,17-20 and 23-29</u> is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1,4-8,11-14,17-20 and 23-29</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/or	r election requirement.						
Application Papers							
9) The specification is objected to by the Examiner.							
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11)☐ The oath or declaration is objected to by the Ex	aminer. Note the attached Office	e Action or form PTO-152.					
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:							
1. Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No							
. — ,	3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list	or the certified copies not receive	ea.					
Attachmont/cl							
Attachment(s) Notice of References Cited (PTO-892)	4) 🔲 Interview Summary	v (PTO-413)					
2) D Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail D	Pate					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Informal I 6) Other:	Patent Application (PTO-152)					
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DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated October 11, 2005.

2. Claims 1, 4-8, 11-14, 17-20, 23-29 are presented for examination.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 1, 8, 14, 20, 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datta et al., U.S. Patent 6393572, hereinafter Datta, in view of Gregorian et al., U.S. Patent 6452425, hereinafter Gregorian.
- 5. In re claim 1, Datta discloses a system [fig.1] comprising:
 - A processing system [master codec 121] comprising memory [col.2, ll.25-39; inherently, storing data requires a memory in the broadest interpretation].
 - A communication adapter [slave codec 122] adapted to be coupled to a transmission medium [lines 131-134, 140-141].
 - Wherein the processing system further comprises:
 - Logic [command processor 230] to receive a sleep message [sleep command]
 from a power management system [digital controller 110] [col.1.57 col.2, l.27;
 sleep command in frame transmitted by 110].

- O Logic [sleep circuit 290] to place the communication adapter in a sleep state [power down sleep mode] in response to the sleep message [col.2, ll.25-51; 121 ceases bit clk 131 to 122].
- O Logic [290, 390 similar] to selectively lower a speed of a clock signal from a first clock speed [bit_clk 131] to a second clock speed [ceased] corresponding with the sleep state [col.4, l.51 col.5, l.17; clock speed corresponding with sleep state is cessation].
- Said communication adapter is adapted to save data local to said communication adapter in said memory prior to transitioning to said sleep state [col.2, ll.25-39].
- 6. Datta did not discuss different protocols.
- 7. Gregorian discloses a system [col.1, ll.4-17] for selectively lowering the speed of the clock from a first clock speed [e.g., F1] to a second speed [e.g., F2], wherein the first clock speed controls the communication adapter [semiconductor chip] to communicate with a transmission medium [lines for transmitters and receivers] according to a first communication protocol having a first data transmission rate [e.g., E3] and the second clock speed controls the communication adapter to communicate with the transmission medium according to a second communication protocol having a second data transmission rate [e.g., DS3] [fig.1,3,5; col.1, ll.16-17; col.2, l.42 col.3, l.25; col.3, l.66 col.4, l.8; setup configuration that selectively lowers the speed of the clock to associated protocol].
- 8. It would have been obvious to one of ordinary skill in the art, having the teachings of
 Datta and Gregorian before him at the time the invention was made, to modify the teachings of
 Datta to include the teachings taught by Gregorian, in order to obtain the processing system that
 comprises logic to selectively lower the speed of the clock from a first clock speed to a second

speed, wherein the first clock speed controls the communication adapter to communicate with a transmission medium according to a first communication protocol and the second clock speed controls the communication adapter to communicate with the transmission medium according to a second communication protocol. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to determine the associated protocol for a particular frequency in a communication environment [Gregorian: col.1, ll.4-54].

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- 9. In re claim 8, Datta and Gregroian disclose each and every limitation as discussed above in reference to claim 1. Datta and Gregorian disclose the system; therefore, Datta and Gregorian disclose an article comprising a storage medium comprising machine-readable instructions [software, firmware, etc.] stored thereon [col.6, ll.6-31] for operating the system.
- 10. In re claims 14 and 20, Datta and Gregroian disclose each and every limitation as discussed above in reference to claim 1. Datta and Gregorian disclose the system; therefore, Datta and Gregorian disclose the method and means thereof for operating the system.
- As to claim 26, Datta discloses the communication adapter that is adapted to retrieve the 11. local data saved in said memory when the communication adapter resumes to a full power state [col.2, ll.25-39].
- As to claim 27, Datta discloses the storage medium that comprises machine readable 12. instructions stored thereon for retrieving the data local to said communication adapter saved in the system memory upon the communication adapter resuming a full power state [col.2, ll.25-39; col.6, Il.6-31].
- As to claim 28, Datta discloses the method that comprises retrieving the data local to the 13. communication adapter saved in the system memory upon the communication adapter resuming a full power state [col.2, ll.25-39].

- 14. As to claim 29, Datta discloses the apparatus comprising means for retrieving the data local to the communication adapter saved in the system memory upon the communication adapter resuming a full power state [col.2, ll.25-39].
- 15. Claims 4-5, 11-12, 17-18, 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datta and Gregorian as applied to claim 1 above, and further in view of Huang et al., U.S. Patent 6407595, hereinafter Huang.
- 16. In re claims 4, 11, 17 and 23, Datta and Gregorian disclose each and every limitation of the claim as discussed above in reference to claim 1. Datta and Gregorian did not discuss the details of responding to the sleep message.
- 17. Huang discloses a system [col.1, ll.4-27] that comprises:
 - Logic to determine the speed of the clock signal [frequency F] in response to a message
 [load signal L; associated with active/sleep] [fig. 1, 4, 7; col. 5, l. 15 col. 6, l. 12; col. 4,
 ll. 27-61; checks F in response to L for appropriate adjustment].
 - Logic to selectively lower the speed of the clock signal [decrease throttling value R to reduce F] if the speed of the clock signal exceeds a predetermined clock speed [FL]
 [fig.1; col.4, ll.51-61].
- 18. It would have been obvious to one of ordinary skill in the art, having the teachings of Huang, Datta and Gregorian before him at the time the invention was made, to modify the teachings of Datta and Gregorian to include the teachings taught by Huang, in order to obtain the processing system that comprises logic to determine the speed of the clock signal in response to the sleep message and logic to selectively lower the speed of the clock signal if the speed of the clock signal exceeds a predetermined clock speed. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to facilitate communication

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[Datta: col.1, 1.5 – col.2, 1.5; Gregorian: col.1, ll.4-54] and control power consumption [Datta: col.2, ll.25-39; Huang: col.1, ll.10-27] in digital systems.

- 19. As to claims 5, 12, 18 and 24, Gregorian discloses an article [col.1, ll.4-17] for:
 - Logic to determine a first communication protocol [e.g., E3; protocol related to speed] being used by the communication adapter [semiconductor chip] [fig.1,3,5; col.2, l.42 col.3, l.25; col.3, l.66 col.4, l.8; determines the protocol via speed].
 - Logic to selectively command the communication adapter to use a second communication protocol [e.g., DS3] if a data rate or clock signal frequency [e.g., F2] associated with the first communication protocol exceeds a threshold [threshold 1] [fig.1,3,5; col.2, 1.42 col.3, 1.25; col.3, 1.66 col.4, 1.8; setup that selectively configures the speed of the clock with associated protocol after determining where frequency lies in relation to threshold].
- 20. Huang discloses an article [col.1, ll.4-27] for:
 - Logic to determine a first speed [frequency F] being used by the communication adapter [graphics chip] in response to a message [load signal L] [fig.4, 7; col.5, l.15 col.6, l.12; col.4, ll.27-61; checks F in response to L for appropriate adjustment].
 - Logic to selectively command the communication adapter to use a second speed
 [throttled F] if a data rate or clock signal frequency [F] exceeds a threshold [FL] [col.4,
 ll.51-61].
- 21. Claims 6, 13, 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datta and Gregorian as applied to claim 1 above, and further in view of Foster, U.S. Patent 6026494.

- 22. Datta and Gregorian disclose each and every limitation of the claim as discussed above in reference to claim 1. Datta and Gregorian did not discuss placing the communication adapter in an auto-sensing state in response to a resume message.
- 23. Foster discloses a system [col.1, ll.6-14] for placing a communication adapter [fig.2; Ethernet transceiver] in an auto-sensing [auto-negotiate] state in response to a resume message [power up after timer2 expires] [col.5, ll.32-62].
- 24. It would have been obvious to one of ordinary skill in the art, having the teachings of Foster, Datta and Gregorian before him at the time the invention was made, to modify the teachings of Datta and Gregorian to include the teachings taught by Foster, in order to obtain the processing system that comprises logic to place the communication adapter in an auto-select state in response to a resume message. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to control power consumption in a communication system [Foster: col.1, ll.6-14].
- 25. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Datta and Gregorian as applied to claim 1 above, and further in view of Greszczuk et al., U.S. Patent 6445730, hereinafter Greszczuk.
- 26. Datta and Gregorian disclose each and every limitation of the claim as discussed above in reference to claim 1. Datta and Gregorian did not discuss details of the interconnection between the communication adapter and processing system.
- 27. Greszczuk discloses a system [col.3, ll.41-60] that comprises a data bus [common telephone line] coupled between the communication adapter [CO transceiver] and the processing system [CPE transceiver], and wherein the processing system further comprises logic to selectively initiate a write command [inherently, some logic in the broadest interpretation is

necessary to communicate] on the data bus addressed to the communication adapter specifying a change in one of a power state in response to a sleep message [power down command] [col.6, 1.12 - col.7, 1.13].

28. It would have been obvious to one of ordinary skill in the art, having the teachings of Datta, Gregorian, and Greszczuk before him at the time the invention was made, to modify the teachings of Datta and Gregorian to include the teachings taught by Greszczuk, in order to obtain the system that comprises a data bus coupled between the communication adapter and the processing system, and wherein the processing system further comprises logic to selectively initiate a write command on the data bus addressed to the communication adapter specifying a change in one of a clock signal frequency and a communication protocol in response to the sleep message. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to rapidly switch from a sleep mode to a full-on condition [Greszczuk: col.3, II.10-20].

Response to Arguments

- 29. Applicant's arguments dated October 11, 2005 have been fully considered but they are not persuasive.
- 30. Applicant's arguments with respect to claims 1, 8, 14, 20, and 26-29 have been considered but are moot in view of the new ground(s) of rejection.
- Applicant alleges that "Gregorian and Huang cannot be properly combined with Datta... to merely change frequency rates or clock speeds in Datta, instead of ceasing a clock signal, would prevent the sleepmode activation in Datta... Huang teaches away from reducing the power consumption by turning off some function inherent in the integrated circuit..." Examiner submits that one of ordinary skill in the art could alter the clock rate associated with the sleep

state in Datta to any other clock rate suitable for the targeted system [different systems may have different clock rates associated with a sleep state] as Datta did not explicitly teach against such modifications [i.e., *Datta is the base reference*]. In effect, one of ordinary skill in the art would alter the clock rate associated with the sleep state in Datta to a non-ceasing clock rate suitable for a graphics chip according to Huang's teaching of motivation in not turning off some function in an integrated circuit.

32. Applicant alleges that "Foster and Greszcuk cannot be properly combined with Datta..."

Examiner submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In the instant case, Examiner submits that the *combined* references teach each and every limitation as discussed in the rejections above.

Conclusion

33. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen November 28, 2005 LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100